CLAIMS

We claim:

1. An analog-to-digital converter, comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals, the pre-amp bank including an array of differential pre-amps, each differential pre-amp of the array of differential pre-amp being offset canceled and reset in response to an HSYNC signal indicating the end of a video line.;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal.

2. The converter according to Claim 1, wherein the folding and interpolating circuit includes a first folding circuit coupled to a second folding circuit, the first folding circuit including active voltage averaging of the set of differential output signals and resistive interpolation.

3. The converter according to Claim 2, wherein the first folding circuit includes a set of first folding sub-blocks, each sub-block of the set of first folding sub-blocks including at least one amplifier section having a number of differential amplifiers having coupled output terminals, each of the number of coupled differential amplifiers coupled to receive one of the differential output signals to provide active voltage averaging.

4. The converter according to Claim 3, wherein each sub-block of the set of first folding sub-blocks includes three amplifier sections having three differential amplifiers each, each of the three amplifier sections receiving sequential ones of the differential output signals with differential output signals received by different ones of the three amplifier sections separated over the set of differential output signals.

5. The converter according to Claim 3, wherein a number of resistive outputs coupled to the output terminals provides resistive interpolation.

6. The converter according to Claim 5, wherein each sub-block provides four differential output signals.

7. The converter according to Claim 3, wherein the first folding circuit includes 12 coupled sub-blocks.

8. The converter according to Claim 2, wherein the second folding circuit includes a number of second folding sub-blocks coupled together, each sub-block of the number of second folding sub-blocks including a number of differential amplifiers having coupled output terminals, each of the number of differential amplifiers coupled to receive signals from the first folding circuit.

9. The converter according to Claim 8, wherein each sub-block includes resistive outputs coupled to the output terminals that provide resistive interpolation.

10. The converter according to Claim 9, wherein each sub-block includes three differential amplifier and provides two output signals to the set of differential folded signals.

11. The converter according to Claim 10, wherein the second folding circuit includes sixteen second folding sub-blocks.

12. The converter according to Claim 1, wherein the comparator bank includes

an array of fine comparators, each comparator of the array of fine comparators coupled to an RS latch, each comparator in the array of fine comparators receiving one of the set of differential folded signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of differential folded signals is positive or negative to the RS latch, and

an array of course comparators, each comparator of the array of course comparators coupled to an RS latch, the array of course comparators receiving one of the set of course differential signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of course differential signals is positive or negative,

wherein the set of digitized fine signals and the set of digitized course signals correspond to outputs of the RS latch coupled to each comparator of the array of fine comparators and the outputs of the RS latch coupled to each comparator of the array of course comparators, respectively.

13. The converter according to Claim 1, wherein the digital encoder includes

a fine decoder that converts the set of digitized fine signals into the least significant bits of the digital signal by determining a number corresponding to the number of the set of digitized fine signals having a first logic level and setting the least significant bits equal to the number, and

a course decoder that converts the set of digitized course signals to the most significant bits of the digital signal by determining a course number indicating the number of the set of digitized course signals having a second logic level.

14. The converter of Claim 13, wherein whether the first logic level is the same or opposite the second logic level is determined by a voting circuit, the voting circuit determining if a region corresponding to the analog input signal is in a rising or falling section.

15. The converter of Claim 13, wherein whether the first logic level is the same or opposite the second logic level is determined by the course number.

16. The converter of Claim 14, wherein the voting circuit inputs one digit from a first extreme of the set of digitized fine signals and two digits from a second extreme opposite the first extreme of the set of digitized fine signals and determines whether the region is a rising or falling section by 2/3 majority vote.

17. The converter of Claim 13, wherein the digital decoder further includes an error correction circuit.

18. The converter of Claim 17, wherein the error correction circuit inputs a determination of whether a region corresponding to the analog input signal is in a rising or falling section, the least significant bit of the course number, and the next to most significant bit of the fine number, determines if there is an agreement of whether the region is a rising or falling section, and adjusts the course number if there is no agreement.

19. The converter of Claim 13, wherein the digital decoder further includes a range correction circuit.

20. The converter of Claim 19, wherein the range correction circuit inputs a first signal of the set of digitized fine signals and a second signal of the set of digitized fine signals, the first signal and the second signal being chosen to be near end points of a range of allowed differential input signals, and the most significant bit of the digital signal, the range correction circuit sets the digital signal at a high extreme value if the first signal indicates a high value of the analog input signal and the most significant bit of the digital signal is not one and sets the digital signal at a low extreme value if the second signal indicates a low value of the analog input signal and the most significant bit of the digital signal is not 0.

21. The converter of Claim 1, wherein the set of differential reference signals includes 32 reference signals and the set of differential output signals includes 32 output signals.

22. The converter of Claim 21, wherein the set of differential folded signals includes 32 differential folded signals.

23. The converter of Claim 22, wherein the set of differential course output signals includes 7 differential course output signals.

24. The converter of Claim 23, wherein the digitized signal includes 8 bits.

25. An analog-to-digital converter, comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals, the pre-amp bank including an array of differential pre-amps, each differential pre-amp of the array of differential pre-amps being offset canceled and reset in response to a random number generated by a random number generator;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal.

26. The converter according to Claim 25, wherein each differential pre-amp of the array of differential pre-amps is a member of a set of pre-amp groups wherein corresponding members of each of the pre-amp groups are offset canceled and reset simultaneously.

27. The converter according to Claim 25, wherein differential output signals from each of the array of differential pre-amps are input to a multiplexer circuit, the multiplexer circuit outputting the set of differential output signals having those differential output signals from those pre-amps in the array of differential pre-amps that are not being offset canceled and reset.

28. The converter according to Claim 25, wherein the folding and interpolating circuit includes a first folding circuit coupled to a second folding circuit, the first folding circuit including active voltage averaging of the set of differential output signals and resistive interpolation.

29. The converter according to Claim 28, wherein the first folding circuit includes a set of first folding sub-blocks, each sub-block of the set of first folding sub-blocks including at least one amplifier section having a number of differential amplifiers having coupled output terminals, each of the number of coupled differential amplifiers coupled to receive one of the differential output signals to provide active voltage averaging.

30. The converter according to Claim 29, wherein each sub-block of the set of first folding sub-blocks includes three amplifier sections having three differential amplifiers each, each of the three amplifier sections receiving sequential ones of the differential output signals with differential output signals received by different ones of the three amplifier sections separated over the set of differential output signals.

31. The converter according to Claim 29, wherein a number of resistive outputs coupled to the output terminals provides resistive interpolation.

32. The converter according to Claim 31, wherein each sub-block provides four differential output signals.

33. The converter according to Claim 29, wherein the first folding circuit includes 12 coupled sub-blocks.

34. The converter according to Claim 28, wherein the second folding circuit includes a number of second folding sub-blocks coupled together, each sub-block of the number of second folding sub-blocks including a number of differential amplifiers having coupled output terminals, each of the number of differential amplifiers coupled to receive signals from the first folding circuit.

35. The converter according to Claim 36, wherein each sub-block includes resistive outputs coupled to the output terminals that provide resistive interpolation.

36. The converter according to Claim 35, wherein each sub-block includes three differential amplifier and provides two output signals to the set of differential folded signals.

37. The converter according to Claim 36, wherein the second folding circuit includes sixteen second folding sub-blocks.

38. The converter according to Claim 25, wherein the comparator bank includes

an array of fine comparators, each comparator of the array of fine comparators coupled to an RS latch, each comparator in the array of fine comparators receiving one of the set of differential folded signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of differential folded signals is positive or negative to the RS latch, and

an array of course comparators, each comparator of the array of course comparators coupled to an RS latch, the array of course comparators receiving one of the set of course differential signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of course differential signals is positive or negative,

wherein the set of digitized fine signals and the set of digitized course signals correspond to outputs of the RS latch coupled to each comparator of the array of fine comparators and the outputs of the RS latch coupled to each comparator of the array of course comparators, respectively.

39. The converter according to Claim 25, wherein the digital encoder includes

a fine decoder that converts the set of digitized fine signals into the least significant bits of the digital signal by determining a number corresponding to the number of the set of digitized fine signals having a first logic level and setting the least significant bits equal to the number, and

a course decoder that converts the set of digitized course signals to the most significant bits of the digital signal by determining a course number

indicating the number of the set of digitized course signals having a second logic level.

40. The converter of Claim 39, wherein whether the first logic level is the same or opposite the second logic level is determined by a voting circuit, the voting circuit determining if a region corresponding to the analog input signal is in a rising or falling section.

41. The converter of Claim 40, wherein the voting circuit inputs one digit from a first extreme of the set of digitized fine signals and two digits from a second extreme opposite the first extreme of the set of digitized fine signals and determines whether the region is a rising or falling section by 2/3 majority vote.

42. The converter of Claim 39, wherein whether the first logic level is the same or opposite the second logic level is determined by the course number.

43. The converter of Claim 39, wherein the digital decoder further includes an error correction circuit.

44. The converter of Claim 43, wherein the error correction circuit inputs a determination of whether a region corresponding to the analog input signal is in a rising or falling section, the least significant bit of the course number, and the next to most significant bit of the fine number, determines if there is an agreement of whether the region is a rising or falling section, and adjusts the course number if there is no agreement.

45. The converter of Claim 39, wherein the digital decoder further includes a range correction circuit.

46. The converter of Claim 45, wherein the range correction circuit inputs a first signal of the set of digitized fine signals and a second signal of the set of digitized fine signals, the first signal and the second signal being chosen to be near end points of a range of allowed differential input signals, and the most significant bit of the digital signal, the range correction circuit sets the digital signal at a high extreme value if the first signal indicates a high value of the analog input signal and the most significant bit of the digital signal is not one and sets the digital signal at a low extreme value if the second signal indicates a low value of the analog input signal and the most significant bit of the digital signal is not 0.

47. The converter of Claim 25, wherein the set of differential reference signals includes 32 reference signals and the set of differential output signals includes 32 output signals.

48. The converter of Claim 25, wherein the set of differential folded signals includes 32 differential folded signals.

49. The converter of Claim 25, wherein the set of differential course output signals includes 7 differential course output signals.

50. The converter of Claim 25, wherein the digitized signal includes 8 bits.

51. An analog-to-digital converter, comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals, the folding and interpolating circuit having a first folding circuit coupled to a second folding circuit, the first folding circuit including active voltage averaging of the set of differential output signals and resistive interpolation;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal.

52. The converter according to Claim 51, wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amp being offset canceled and reset in response to an HSYNC signal indicating the end of a video line.

53. The converter according to Claim 51, wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amps being offset canceled and reset in response to a random number generated by a random number generator.

54. The converter according to Claim 53, wherein each differential pre-amp of the array of differential pre-amps is a member of a set of pre-amp groups wherein corresponding members of each of the pre-amp groups are offset canceled and reset simultaneously.

55. The converter according to Claim 53, wherein differential output signals from each of the array of differential pre-amps are input to a multiplexer circuit, the multiplexer circuit outputting the set of differential output signals having those differential output signals from those pre-amps in the array of differential pre-amps that are not being offset canceled and reset.

56. The converter according to Claim 51, wherein the first folding circuit includes a set of first folding sub-blocks, each sub-block of the set of first folding sub-blocks including at least one amplifier section having a number of differential amplifiers having coupled output terminals, each of the number of coupled differential amplifiers coupled to receive one of the differential output signals to provide active voltage averaging.

57. The converter according to Claim 56, wherein each sub-block of the set of first folding sub-blocks includes three amplifier sections having three differential amplifiers each, each of the three amplifier sections receiving sequential ones of the differential output signals with differential output signals received by different ones of the three amplifier sections separated over the set of differential output signals.

58. The converter according to Claim 56, wherein a number of resistive outputs coupled to the output terminals provides resistive interpolation.

59. The converter according to Claim 58, wherein each sub-block provides four differential output signals.

60. The converter according to Claim 56, wherein the first folding circuit includes 12 coupled sub-blocks.

61. The converter according to Claim 55, wherein the second folding circuit includes a number of second folding sub-blocks coupled together, each sub-block of the number of second folding sub-blocks including a number of differential amplifiers having coupled output terminals, each of the number of differential amplifiers coupled to receive signals from the first folding circuit.

62. The converter according to Claim 61, wherein each sub-block includes resistive outputs coupled to the output terminals that provide resistive interpolation.

63. The converter according to Claim 62, wherein each sub-block includes three differential amplifier and provides two output signals to the set of differential folded signals.

64. The converter according to Claim 63, wherein the second folding circuit includes sixteen second folding sub-blocks.

65. The converter according to Claim 51, wherein the comparator bank includes

an array of fine comparators, each comparator of the array of fine comparators coupled to an RS latch, each comparator in the array of fine comparators receiving one of the set of differential folded signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of differential folded signals is positive or negative to the RS latch, and

an array of course comparators, each comparator of the array of course comparators coupled to an RS latch, the array of course comparators receiving one of the set of course differential signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of course differential signals is positive or negative,

wherein the set of digitized fine signals and the set of digitized course signals correspond to outputs of the RS latch coupled to each comparator of the array of fine comparators and the outputs of the RS latch coupled to each comparator of the array of course comparators, respectively.

66. The converter according to Claim 51, wherein the digital encoder includes

a fine decoder that converts the set of digitized fine signals into the least significant bits of the digital signal by determining a number corresponding to the number of the set of digitized fine signals having a first logic level and setting the least significant bits equal to the number, and

a course decoder that converts the set of digitized course signals to the most significant bits of the digital signal by determining a course number indicating the number of the set of digitized course signals having a second logic level.

67. The converter of Claim 66, wherein whether the first logic level is the same or opposite the second logic level is determined by a voting circuit, the voting circuit determining if a region corresponding to the analog input signal is in a rising or falling section.

68. The converter of Claim 67, wherein the voting circuit inputs one digit from a first extreme of the set of digitized fine signals and two digits from a second extreme opposite the first extreme of the set of digitized fine signals and determines whether the region is a rising or falling section by 2/3 majority vote.

69. The converter of Claim 66, wherein whether the first logic level is the same or opposite the second logic level is determined by the course number.

70. The converter of Claim 66, wherein the digital decoder further includes an error correction circuit.

71. The converter of Claim 70, wherein the error correction circuit inputs a determination of whether a region corresponding to the analog input signal is in a rising or falling section, the least significant bit of the course number, and the next to most significant bit of the fine number, determines if there is an agreement of whether the region is a rising or falling section, and adjusts the course number if there is no agreement.

72. The converter of Claim 66, wherein the digital decoder further includes a range correction circuit.

73. The converter of Claim 72, wherein the range correction circuit inputs a first signal of the set of digitized fine signals and a second signal of the set of digitized fine signals, the first signal and the second signal being chosen to be near end points of a range of allowed differential input signals, and the most significant bit of the digital signal, the range correction circuit sets the digital signal at a high extreme value if the first signal indicates a high value of the analog input signal and the most significant bit of the digital signal is not one and sets the digital signal at a low extreme value if the second signal indicates a low value of the analog input signal and the most significant bit of the digital signal is not 0.

74. The converter of Claim 51, wherein the set of differential reference signals includes 32 reference signals and the set of differential output signals includes 32 output signals.

75. The converter of Claim 74, wherein the set of differential folded signals includes 32 differential folded signals.

76. The converter of Claim 75, wherein the set of differential course output signals includes 7 differential course output signals.

77. The converter of Claim 76, wherein the digitized signal includes 8 bits.

78. An analog-to-digital converter, comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals, the comparator bank including

an array of fine comparators, each comparator of the array of fine comparators coupled to an RS latch, each comparator in the array of fine comparators receiving one of the set of differential folded signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of differential folded signals is positive or negative to the RS latch, and

an array of course comparators, each comparator of the array of course comparators coupled to an RS latch, the array of course comparators receiving one of the set of course differential signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of course differential signals is positive or negative,

wherein the set of digitized fine signals and the set of digitized course signals correspond to outputs of the RS latch coupled to each comparator of the array of fine comparators and the outputs of the RS latch coupled to each comparator of the array of course comparators, respectively; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal.

79. The converter according to Claim 78, wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amp being offset canceled and reset in response to an HSYNC signal indicating the end of a video line.

80. The converter according to Claim 78, wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amps being

offset canceled and reset in response to a random number generated by a random number generator.

81. The converter according to Claim 80, wherein each differential pre-amp of the array of differential pre-amps is a member of a set of pre-amp groups wherein corresponding members of each of the pre-amp groups are offset canceled and reset simultaneously.

82. The converter according to Claim 80, wherein differential output signals from each of the array of differential pre-amps are input to a multiplexer circuit, the multiplexer circuit outputting the set of differential output signals having those differential output signals from those pre-amps in the array of differential pre-amps that are not being offset canceled and reset.

83. The converter according to Claim 78, wherein the folding and interpolating circuit includes a first folding circuit coupled to a second folding circuit, the first folding circuit including active voltage averaging of the set of differential output signals and resistive interpolation.

84. The converter according to Claim 83, wherein the first folding circuit includes a set of first folding sub-blocks, each sub-block of the set of first folding sub-blocks including at least one amplifier section having a number of differential amplifiers having coupled output terminals, each of the number of coupled differential amplifiers coupled to receive one of the differential output signals to provide active voltage averaging.

85. The converter according to Claim 84, wherein each sub-block of the set of first folding sub-blocks includes three amplifier sections having three differential amplifiers each, each of the three amplifier sections receiving sequential ones of the differential output signals with differential output signals received by different ones of the three amplifier sections separated over the set of differential output signals.

86. The converter according to Claim 84, wherein a number of resistive outputs coupled to the output terminals provides resistive interpolation.

87. The converter according to Claim 86, wherein each sub-block provides four differential output signals.

88. The converter according to Claim 84, wherein the first folding circuit includes 12 coupled sub-blocks.

89. The converter according to Claim 83, wherein the second folding circuit includes a number of second folding sub-blocks coupled together, each sub-block of the number of second folding sub-blocks including a number of differential amplifiers having coupled output terminals, each of the number of differential amplifiers coupled to receive signals from the first folding circuit.

90. The converter according to Claim 89, wherein each sub-block includes resistive outputs coupled to the output terminals that provide resistive interpolation.

91. The converter according to Claim 90, wherein each sub-block includes three differential amplifier and provides two output signals to the set of differential folded signals.

92. The converter according to Claim 91, wherein the second folding circuit includes sixteen second folding sub-blocks.

93. The converter according to Claim 78, wherein the digital encoder includes

a fine decoder that converts the set of digitized fine signals into the least significant bits of the digital signal by determining a number corresponding to the number of the set of digitized fine signals having a first logic level and setting the least significant bits equal to the number, and

a course decoder that converts the set of digitized course signals to the most significant bits of the digital signal by determining a course number indicating the number of the set of digitized course signals having a second logic level.

94. The converter of Claim 93, wherein whether the first logic level is the same or opposite the second logic level is determined by a voting circuit, the voting circuit determining if a region corresponding to the analog input signal is in a rising or falling section.

95. The converter of Claim 94, wherein the voting circuit inputs one digit from a first extreme of the set of digitized fine signals and two digits from a second extreme opposite the first extreme of the set of digitized fine signals and determines whether the region is a rising or falling section by 2/3 majority vote.

96. The converter of Claim 93, wherein whether the first logic level is the same or opposite the second logic level is determined by the course number.

97. The converter of Claim 93, wherein the digital decoder further includes an error correction circuit.

98. The converter of Claim 97, wherein the error correction circuit inputs a determination of whether a region corresponding to the analog input signal is in a rising or falling section, the least significant bit of the course number, and the next to most significant bit of the fine number, determines if there is an agreement of whether the region is a rising or falling section, and adjusts the course number if there is no agreement.

99. The converter of Claim 93, wherein the digital decoder further includes a range correction circuit.

100. The converter of Claim 99, wherein the range correction circuit inputs a first signal of the set of digitized fine signals and a second signal of the set of digitized fine signals, the first signal and the second signal being chosen to be near end points of a range of allowed differential input signals, and the most significant bit of the digital signal, the range correction circuit sets the digital signal at a high extreme value if the first signal indicates a high value of the analog input signal and the most significant bit of the digital signal is not one and sets the digital signal at a low extreme value if the second signal indicates a low value of the analog input signal and the most significant bit of the digital signal is not 0.

101. The converter of Claim 78, wherein the set of differential reference signals includes 32 reference signals and the set of differential output signals includes 32 output signals.

102. The converter of Claim 101, wherein the set of differential folded signals includes 32 differential folded signals.

103. The converter of Claim 102, wherein the set of differential course output signals includes 7 differential course output signals.

104. The converter of Claim 103, wherein the digitized signal includes 8 bits.

105. An analog-to-digital converter, comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal, the digital encoder including

a fine decoder that converts the set of digitized fine signals into the least significant bits of the digital signal by determining a number corresponding to the number of the set of digitized fine signals having a first logic level and setting the least significant bits equal to the number, and

a course decoder that converts the set of digitized course signals to the most significant bits of the digital signal by determining a course number indicating the number of the set of digitized course signals having a second logic level.

106. The converter according to Claim 105, wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amp being offset canceled and reset in response to an HSYNC signal indicating the end of a video line.

107. The converter according to Claim 105, wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amps being offset canceled and reset in response to a random number generated by a random number generator.

108. The converter according to Claim 107, wherein each differential pre-amp of the array of differential pre-amps is a member of a set of pre-amp groups wherein corresponding members of each of the pre-amp groups are offset canceled and reset simultaneously.

109. The converter according to Claim 107, wherein differential output signals from each of the array of differential pre-amps are input to a multiplexer circuit, the multiplexer circuit outputting the set of differential output signals having those differential output signals from those pre-amps in the array of differential pre-amps that are not being offset canceled and reset.

110. The converter according to Claim 105, wherein the folding and interpolating circuit includes a first folding circuit coupled to a second folding circuit, the first folding circuit including active voltage averaging of the set of differential output signals and resistive interpolation.

111. The converter according to Claim 110, wherein the first folding circuit includes a set of first folding sub-blocks, each sub-block of the set of first folding sub-blocks including at least one amplifier section having a number of differential amplifiers having coupled output terminals, each of the number of coupled differential amplifiers coupled to receive one of the differential output signals to provide active voltage averaging.

112. The converter according to Claim 111, wherein each sub-block of the set of first folding sub-blocks includes three amplifier sections having three differential amplifiers each, each of the three amplifier sections receiving sequential ones of the differential output signals with differential output signals received by different ones of the three amplifier sections separated over the set of differential output signals.

113. The converter according to Claim 111, wherein a number of resistive outputs coupled to the output terminals provides resistive interpolation.

114. The converter according to Claim 113, wherein each sub-block provides four differential output signals.

115. The converter according to Claim 111, wherein the first folding circuit includes 12 coupled sub-blocks.

116. The converter according to Claim 110, wherein the second folding circuit includes a number of second folding sub-blocks coupled together, each sub-block of the number of second folding sub-blocks including a number of differential amplifiers having coupled output terminals, each of the number of differential amplifiers coupled to receive signals from the first folding circuit.

117. The converter according to Claim 116, wherein each sub-block includes resistive outputs coupled to the output terminals that provide resistive interpolation.

118. The converter according to Claim 117, wherein each sub-block includes three differential amplifier and provides two output signals to the set of differential folded signals.

119. The converter according to Claim 118, wherein the second folding circuit includes sixteen second folding sub-blocks.

120. The converter according to Claim 105, wherein the comparator bank includes

an array of fine comparators, each comparator of the array of fine comparators coupled to an RS latch, each comparator in the array of fine comparators receiving one of the set of differential folded signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of differential folded signals is positive or negative to the RS latch, and

an array of course comparators, each comparator of the array of course comparators coupled to an RS latch, the array of course comparators receiving one of the set of course differential signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of course differential signals is positive or negative,

wherein the set of digitized fine signals and the set of digitized course signals correspond to outputs of the RS latch coupled to each comparator of the array of fine comparators and the outputs of the RS latch coupled to each comparator of the array of course comparators, respectively.

121. The converter of Claim 105, wherein whether the first logic level is the same or opposite the second logic level is determined by a voting circuit, the voting circuit determining if a region corresponding to the analog input signal is in a rising or falling section.

122. The converter of Claim 121, wherein the voting circuit inputs one digit from a first extreme of the set of digitized fine signals and two digits from a second extreme opposite the first extreme of the set of digitized fine signals and determines whether the region is a rising or falling section by 2/3 majority vote.

123. The converter of Claim 120, wherein whether the first logic level is the same or opposite the second logic level is determined by the course number.

124. The converter of Claim 120, wherein the digital decoder further includes an error correction circuit.

125. The converter of Claim 124, wherein the error correction circuit inputs a determination of whether a region corresponding to the analog input signal is in a rising or falling section, the least significant bit of the course number, and the next to most significant bit of the fine number, determines if there is an agreement of whether the region is a rising or falling section, and adjusts the course number if there is no agreement.

126. The converter of Claim 120, wherein the digital decoder further includes a range correction circuit.

127. The converter of Claim 126, wherein the range correction circuit inputs a first signal of the set of digitized fine signals and a second signal of the set of digitized fine signals, the first signal and the second signal being chosen to be near end points of a range of allowed differential input signals, and the most significant bit of the digital signal, the range correction circuit sets the digital signal at a high extreme value if the first signal indicates a high value of the analog input signal and the most significant bit of the digital signal is not one and sets the digital signal at a low extreme value if the second signal indicates a low value of the analog input signal and the most significant bit of the digital signal is not 0.

128. The converter of Claim 105, wherein the set of differential reference signals includes 32 reference signals and the set of differential output signals includes 32 output signals.

129. The converter of Claim 128, wherein the set of differential folded signals includes 32 differential folded signals.

130. The converter of Claim 129, wherein the set of differential course output signals includes 7 differential course output signals.

131. The converter of Claim 130, wherein the digitized signal includes 8 bits.

132. A phase-locked-loop, comprising:

a phase detector coupled to receive a reference signal having a frequency and a comparison signal, the phase detector providing a phase detection signal in response to a comparison between the reference signal and the comparison signal;

a reference generator coupled to receive the phase detection signal from the phase detector, the reference generator providing an output signal having a frequency related to the phase detection signal; and

a programmable Div/N circuit coupled to receive the output signal, the programmable Div/N circuit generating the comparison signal in response to the output signal, the frequency of the comparison signal being related to the frequency of the output signal by a factor related to a value stored in a storage register.

133. The phase-locked-loop of Claim 132, wherein the programmable Div/N circuit includes

a counter coupled to the storage register so that a count value stored in the counter is initialized with the value when a zero signal indicates that the counter value is zero, the count value being decremented on each cycle of the output signal;

a decode circuit coupled to the counter to receive the count value, the decode circuit detecting when the count value is zero; and

a flip-flop coupled to the decode circuit so that the flip-flop outputs a logic high whenever the decode circuit detects that the count value is zero, the output signal from the flip-flop providing the comparison signal and the zero signal.

134. A reference and bias voltage generator, comprising:

a digital-to-analog converter coupled to receive a reference value from a gain register and a band-gap voltage, the digital-to-analog converter outputting a scaled bandgap voltage relative to the band-gap voltage in response to the reference value;

a current digital-to-analog converter coupled to receive the scaled bandgap voltage from the digital-to-analog converter, the current digital-to-analog converter outputting a bias voltage signal relative to the voltage reference signal and an offset value from an offset register.

135. The generator of Claim 134, wherein the digital-to-analog converter includes an amplifier coupled to receive the band-gap voltage, a current circuit coupled to the amplifier to convert the band-gap voltage to a current signal, and an array of current mirrors coupled to mirror the current signal, each current mirror of the array of current mirrors coupled to a multiplexer which routs the current signal to a resistor ladder or to a ground voltage based on individual bits of the reference value stored in the gain register, the resistor ladder supplying the scaled bandgap voltage.

136. The generator of Claim 135, wherein the scaled bandgap voltage supplies a voltage reference signal.

137. The generator of Claim 134, wherein the current digital-to-analog converter includes an amplifier coupled to receive the scaled bandgap voltage from the digital-to-analog converter, a current circuit coupled to the amplifier to convert the band-gap voltage to a current signal, and an array of current mirrors coupled to mirror the current signal, each current mirror of the array of current mirrors coupled to a multiplexer which routs the current signal to a resistor ladder or to a ground voltage based on individual bits of the offset value stored in the offset register.

138. The generator of Claim 137, wherein the current digital-to-analog converter includes a separate current mirror to produce the voltage reference signal within the current digital-to-analog converter.

139. A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein the phase-locked-loop, comprises:

a phase detector coupled to receive a reference signal having a frequency and a comparison signal, the phase detector providing a phase detection signal in response to a comparison between the reference signal and the comparison signal;

a reference generator coupled to receive the phase detection signal from the phase detector, the reference generator providing an output signal having a frequency related to the phase detection signal; and

a programmable Div/N circuit coupled to receive the output signal, the programmable Div/N circuit generating the comparison signal in response to the output signal, the frequency of the comparison signal being related to the frequency of the output signal by a factor related to a value stored in a storage register.

140. The digitizer according to Claim 139, wherein the programmable Div/N circuit includes:

a counter coupled to the storage register so that a count value stored in the counter is initialized with the value when a zero signal indicates that the counter value is zero, the count value being decremented on each cycle of the output signal;

a decode circuit coupled to the counter to receive the count value, the decode circuit detecting when the count value is zero; and

a flip-flop coupled to the decode circuit so that the flip-flop outputs a logic high whenever the decode circuit detects that the count value is zero, the output signal from the flip-flop providing the comparison signal and the zero signal.

141. A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes a reference and bias voltage generator, the reference and bias voltage generator, comprising:

a digital-to-analog converter coupled to receive a reference value from a gain register and a band-gap voltage, the digital-to-analog converter outputting a scaled bandgap voltage relative to the band-gap voltage in response to the reference value;

a current digital-to-analog converter coupled to receive the scaled bandgap voltage from the digital-to-analog converter, the current digital-to-analog converter outputting a bias voltage signal relative to the voltage reference signal and an offset value from an offset register.

142. The digitizer of Claim 141, wherein the digital-to-analog converter includes an amplifier coupled to receive the band-gap voltage, a current circuit coupled to the amplifier to convert the band-gap voltage to a current signal, and an array of current mirrors coupled to mirror the current signal, each current mirror of the array of current mirrors coupled to a multiplexer which routs the current signal to a resistor ladder or to a ground voltage based on individual bits of the reference value stored in the gain register, the resistor ladder supplying the scaled bandgap voltage.

143. The digitizer of Claim 142, wherein the scaled bandgap voltage supplies a voltage reference signal.

144. The digitizer of Claim 141, wherein the current digital-to-analog converter includes an amplifier coupled to receive the scaled bandgap voltage from the digital-to-analog converter, a current circuit coupled to the amplifier to convert the band-gap voltage to a current signal, and an array of current mirrors coupled to mirror the current signal, each current mirror of the array of current mirrors coupled to a multiplexer which routs the current signal to a resistor ladder or to a ground voltage based on individual bits of the offset value stored in the offset register.

145. The generator of Claim 144, wherein the current digital-to-analog converter includes a separate current mirror to produce the voltage reference signal within the current digital-to-analog converter.

146. A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein a phase between the sampling clock frequency and the horizontal sync signal is controlled by a phase value stored in a phase register and the timing generator circuit includes a phase adapter circuit that controls the sampling of the horizontal sync signal.

147. The digitizer according to Claim 146, wherein the timing generator circuit further includes:

a first circuit to sample the horizontal sync signal with a phase-zero signal to form a local horizontal sync signal;

a second circuit to sample the local horizontal sync signal with an adapted signal from the phase adapter circuit; and

an output circuit coupled to generate the synchronized horizontal sync signal.

148. The digitizer according to Claim 147, wherein the phase adapter circuit includes a logic circuit that samples the phase value stored in the phase register and determines if a sampling phase is in a first and fourth quadrant or a second and third quadrant with respect to the horizontal sync signal and setting the adapted signal to the same phase as the sampling clock signal or to the complementary phase as the sampling clock signal accordingly.

149. A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amp being offset canceled and reset in response to an HSYNC signal indicating the end of a video line.

150. A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amps being offset canceled and reset in response to a random number generated by a random number generator.

151. The digitizer according to Claim 150, wherein each differential pre-amp of the array of differential pre-amps is a member of a set of pre-amp groups wherein corresponding members of each of the pre-amp groups are offset canceled and reset simultaneously.

152. The digitizer according to Claim 150, wherein differential output signals from each of the array of differential pre-amps are input to a multiplexer circuit, the multiplexer circuit outputting the set of differential output signals having those differential output signals from those pre-amps in the array of differential pre-amps that are not being offset canceled and reset.

153. A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the folding and interpolating circuit includes a first folding circuit coupled to a second folding circuit, the first folding circuit including active voltage averaging of the set of differential output signals and resistive interpolation.

154. The digitizer according to Claim 153, wherein the first folding circuit includes a set of first folding sub-blocks, each sub-block of the set of first folding sub-blocks including at least one amplifier section having a number of differential amplifiers having coupled output terminals, each of the number of coupled differential amplifiers coupled to receive one of the differential output signals to provide active voltage averaging.

155. The digitizer according to Claim 154, wherein each sub-block of the set of first folding sub-blocks includes three amplifier sections having three differential amplifiers each, each of the three amplifier sections receiving sequential ones of the differential output signals with differential output signals received by different ones of the three amplifier sections separated over the set of differential output signals.

156. The digitizer according to Claim 154, wherein a number of resistive outputs coupled to the output terminals provides resistive interpolation.

157. The digitizer according to Claim 156, wherein each sub-block provides four differential output signals.

158. The digitizer according to Claim 154, wherein the first folding circuit includes 12 coupled sub-blocks.

159. The digitizer according to Claim 153, wherein the second folding circuit includes a number of second folding sub-blocks coupled together, each sub-block of the number of second folding sub-blocks including a number of differential amplifiers having coupled output terminals, each of the number of differential amplifiers coupled to receive signals from the first folding circuit.

160. The digitizer according to Claim 159, wherein each sub-block includes resistive outputs coupled to the output terminals that provide resistive interpolation.

161. The digitizer according to Claim 160, wherein each sub-block includes three differential amplifier and provides two output signals to the set of differential folded signals.

162. The digitizer according to Claim 160, wherein the second folding circuit includes sixteen second folding sub-blocks.

163. A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the comparator bank includes

an array of fine comparators, each comparator of the array of fine comparators coupled to an RS latch, each comparator in the array of fine comparators receiving one of the set of differential folded signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of differential folded signals is positive or negative to the RS latch, and

an array of course comparators, each comparator of the array of course comparators coupled to an RS latch, the array of course comparators receiving one of the set of course differential signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of course differential signals is positive or negative,

wherein the set of digitized fine signals and the set of digitized course signals correspond to outputs of the RS latch coupled to each comparator of the array of fine comparators and the outputs of the RS latch coupled to each comparator of the array of course comparators, respectively.

164. A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the digital encoder includes

a fine decoder that converts the set of digitized fine signals into the least significant bits of the digital signal by determining a number corresponding to the number of the set of digitized fine signals having a first logic level and setting the least significant bits equal to the number, and

a course decoder that converts the set of digitized course signals to the most significant bits of the digital signal by determining a course number indicating the number of the set of digitized course signals having a second logic level.

165. The digitizer of Claim 164, wherein whether the first logic level is the same or opposite the second logic level is determined by a voting circuit, the voting circuit determining if a region corresponding to the analog input signal is in a rising or falling section.

166. The digitizer of Claim 165, wherein the voting circuit inputs one digit from a first extreme of the set of digitized fine signals and two digits from a second extreme opposite the first extreme of the set of digitized fine signals and determines whether the region is a rising or falling section by 2/3 majority vote.

167. The digitizer of Claim 164, wherein whether the first logic level is the same or opposite the second logic level is determined by the course number.

168. The digitizer of Claim 164, wherein the digital decoder further includes an error correction circuit.

169. The digitizer of Claim 168, wherein the error correction circuit inputs a determination of whether a region corresponding to the analog input signal is in a rising or falling section, the least significant bit of the course number, and the next to most significant bit of the fine number, determines if there is an agreement of whether the region is a rising or falling section, and adjusts the course number if there is no agreement.

170. The digitizer of Claim 164, wherein the digital decoder further includes a range correction circuit.

171. The digitizer of Claim 170, wherein the range correction circuit inputs a first signal of the set of digitized fine signals and a second signal of the set of digitized fine signals, the first signal and the second signal being chosen to be near end points of a range of allowed differential input signals, and the most significant bit of the digital signal, the range correction circuit sets the digital signal at a high extreme value if the first signal indicates a high value of the analog input signal and the most significant bit of the digital signal is not one and sets the digital signal at a low extreme value if the second signal indicates a low value of the analog input signal and the most significant bit of the digital signal is not 0.

172. A graphics digitizer, comprising:

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the set of differential reference signals includes 32 reference signals and the set of differential output signals includes 32 output signals.

173. The digitizer of Claim 172, wherein the set of differential folded signals includes 32 differential folded signals.

174. The digitizer of Claim 173, wherein the set of differential course output signals includes 7 differential course output signals.

175. The digitizer of Claim 174, wherein the digitized signal includes 8 bits.

176. A digital display unit, comprising:

an array of pixels;

a digital pixel controller coupled to the array of pixels, the digital pixel controller capable of turning on pixels in the array of pixels in response to a set of digital video signals; and

a graphics digitizer coupled to the digital pixel controller, the graphics digitizer supplying the set of digital video signals in response to a set of analog video signals, the graphics digitizer including

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein the phase-locked-loop, comprises:

a phase detector coupled to receive a reference signal having a frequency and a comparison signal, the phase detector providing a phase detection signal in response to a comparison between the reference signal and the comparison signal;

a reference generator coupled to receive the phase detection signal from the phase detector, the reference generator providing an output signal having a frequency related to the phase detection signal; and

a programmable Div/N circuit coupled to receive the output signal, the programmable Div/N circuit generating the comparison signal in response to the output signal, the frequency of the comparison signal being related to the frequency of the output signal by a factor related to a value stored in a storage register.

177. The digital display unit according to Claim 176, wherein the programmable Div/N circuit includes:

a counter coupled to the storage register so that a count value stored in the counter is initialized with the value when a zero signal indicates that the counter value is zero, the count value being decremented on each cycle of the output signal;

a decode circuit coupled to the counter to receive the count value, the decode circuit detecting when the count value is zero; and

a flip-flop coupled to the decode circuit so that the flip-flop outputs a logic high whenever the decode circuit detects that the count value is zero, the output signal from the flip-flop providing the comparison signal and the zero signal.

178. A digital display unit, comprising:

an array of pixels;

a digital pixel controller coupled to the array of pixels, the digital pixel controller capable of turning on pixels in the array of pixels in response to a set of digital video signals; and

a graphics digitizer coupled to the digital pixel controller, the graphics digitizer supplying the set of digital video signals in response to a set of analog video signals, the graphics digitizer including

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes a reference and bias voltage generator, the reference and bias voltage generator, comprising:

a digital-to-analog converter coupled to receive a reference value from a gain register and a band-gap voltage, the digital-to-analog converter outputting a scaled bandgap voltage relative to the band-gap voltage in response to the reference value;

a current digital-to-analog converter coupled to receive the scaled bandgap voltage from the digital-to-analog converter, the current digital-to-analog converter outputting a bias voltage signal relative to the voltage reference signal and an offset value from an offset register.

179. The digital display unit of Claim 178, wherein the digital-to-analog converter includes an amplifier coupled to receive the band-gap voltage, a current circuit coupled to the amplifier to convert the band-gap voltage to a current signal, and an array of current mirrors coupled to mirror the current signal, each current mirror of the array of current mirrors coupled to a multiplexer which routs the current signal to a resistor ladder or to a ground voltage based on individual bits of the reference value stored in the gain register, the resistor ladder supplying the scaled bandgap voltage.

180. The digital display unit of Claim 179, wherein the scaled bandgap voltage supplies a voltage reference signal.

181. The digital display unit of Claim 178, wherein the current digital-to-analog converter includes an amplifier coupled to receive the scaled bandgap voltage from the digital-to-analog converter, a current circuit coupled to the amplifier to convert the band-gap voltage to a current signal, and an array of current mirrors coupled to mirror the current signal, each current mirror of the array of current mirrors coupled to a multiplexer which routs the current signal to a resistor ladder or to a ground voltage based on individual bits of the offset value stored in the offset register.

182. The digital display unit of Claim 181, wherein the current digital-to-analog converter includes a separate current mirror to produce the voltage reference signal within the current digital-to-analog converter.

183. A digital display unit, comprising:

an array of pixels;

a digital pixel controller coupled to the array of pixels, the digital pixel controller capable of turning on pixels in the array of pixels in response to a set of digital video signals; and

a graphics digitizer coupled to the digital pixel controller, the graphics digitizer supplying the set of digital video signals in response to a set of analog video signals, the graphics digitizer including

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein a phase between the sampling clock frequency and the horizontal sync signal is controlled by a phase value stored in a phase register and the timing generator circuit includes a phase adapter circuit that controls the sampling of the horizontal sync signal.

184. The digital display unit according to Claim 183, wherein the timing generator circuit further includes:

a first circuit to sample the horizontal sync signal with a phase-zero signal to form a local horizontal sync signal;

a second circuit to sample the local horizontal sync signal with an adapted signal from the phase adapter circuit; and

an output circuit coupled to generate the synchronized horizontal sync signal.

185. The digital display unit according to Claim 184, wherein the phase adapter circuit includes a logic circuit that samples the phase value stored in the phase register and determines if a sampling phase is in a first and fourth quadrant or a second and third quadrant with respect to the horizontal sync signal and setting the adapted signal to the same phase as the sampling clock signal or to the complementary phase as the sampling clock signal accordingly.

186. A digital display unit, comprising:

an array of pixels;

a digital pixel controller coupled to the array of pixels, the digital pixel controller capable of turning on pixels in the array of pixels in response to a set of digital video signals; and

a graphics digitizer coupled to the digital pixel controller, the graphics digitizer supplying the set of digital video signals in response to a set of analog video signals, the graphics digitizer including

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amp being offset canceled and reset in response to an HSYNC signal indicating the end of a video line.

187. A digital display unit, comprising:

an array of pixels;

a digital pixel controller coupled to the array of pixels, the digital pixel controller capable of turning on pixels in the array of pixels in response to a set of digital video signals; and

a graphics digitizer coupled to the digital pixel controller, the graphics digitizer supplying the set of digital video signals in response to a set of analog video signals, the graphics digitizer including

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the pre-amp bank includes an array of differential pre-amps, each differential pre-amp of the array of differential pre-amps being offset canceled and reset in response to a random number generated by a random number generator.

188. The digital display unit according to Claim 187, wherein each differential pre-amp of the array of differential pre-amps is a member of a set of pre-amp groups wherein corresponding members of each of the pre-amp groups are offset canceled and reset simultaneously.

189. The digital display unit according to Claim 187, wherein differential output signals from each of the array of differential pre-amps are input to a multiplexer circuit, the multiplexer circuit outputting the set of differential output signals having those differential output signals from those pre-amps in the array of differential pre-amps that are not being offset canceled and reset.

190. A digital display unit, comprising:

an array of pixels;

a digital pixel controller coupled to the array of pixels, the digital pixel controller capable of turning on pixels in the array of pixels in response to a set of digital video signals; and

a graphics digitizer coupled to the digital pixel controller, the graphics digitizer supplying the set of digital video signals in response to a set of analog video signals, the graphics digitizer including

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the folding and interpolating circuit includes a first folding circuit coupled to a second folding circuit, the first folding circuit including active voltage averaging of the set of differential output signals and resistive interpolation.

191. The digital display unit according to Claim 190, wherein the first folding circuit includes a set of first folding sub-blocks, each sub-block of the set of first folding sub-blocks including at least one amplifier section having a number of differential amplifiers having coupled output terminals, each of the number of coupled differential amplifiers coupled to receive one of the differential output signals to provide active voltage averaging.

192. The digital display unit according to Claim 191, wherein each sub-block of the set of first folding sub-blocks includes three amplifier sections having three differential amplifiers each, each of the three amplifier sections receiving sequential ones of the differential output signals with differential output signals received by different ones of the three amplifier sections separated over the set of differential output signals.

193. The digital display unit according to Claim 191, wherein a number of resistive outputs coupled to the output terminals provides resistive interpolation.

194. The digital display unit according to Claim 193, wherein each sub-block provides four differential output signals.

195. The digital display unit according to Claim 191, wherein the first folding circuit includes 12 coupled sub-blocks.

196. The digital display unit according to Claim 190, wherein the second folding circuit includes a number of second folding sub-blocks coupled together, each sub-block of the number of second folding sub-blocks including a number of differential amplifiers having coupled output terminals, each of the number of differential amplifiers coupled to receive signals from the first folding circuit.

197. The digital display unit according to Claim 196, wherein each sub-block includes resistive outputs coupled to the output terminals that provide resistive interpolation.

198. The digital display unit according to Claim 197, wherein each sub-block includes three differential amplifier and provides two output signals to the set of differential folded signals.

199. The digital display unit according to Claim 197, wherein the second folding circuit includes sixteen second folding sub-blocks.

200. A digital display unit, comprising:

an array of pixels;

a digital pixel controller coupled to the array of pixels, the digital pixel controller capable of turning on pixels in the array of pixels in response to a set of digital video signals; and

a graphics digitizer coupled to the digital pixel controller, the graphics digitizer supplying the set of digital video signals in response to a set of analog video signals, the graphics digitizer including

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the comparator bank includes

an array of fine comparators, each comparator of the array of fine comparators coupled to an RS latch, each comparator in the array of fine comparators receiving one of the set of differential folded signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of differential folded signals is positive or negative to the RS latch, and

an array of course comparators, each comparator of the array of course comparators coupled to an RS latch, the array of course comparators receiving one of the set of course differential signals and outputting a binary digit and a complementary binary digit indicating whether the one of the set of course differential signals is positive or negative,

wherein the set of digitized fine signals and the set of digitized course signals correspond to outputs of the RS latch coupled to each comparator of the array of fine comparators and the outputs of the RS latch coupled to each comparator of the array of course comparators, respectively.

201. A digital display unit, comprising:

an array of pixels;

a digital pixel controller coupled to the array of pixels, the digital pixel controller capable of turning on pixels in the array of pixels in response to a set of digital video signals; and

a graphics digitizer coupled to the digital pixel controller, the graphics digitizer supplying the set of digital video signals in response to a set of analog video signals, the graphics digitizer including

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the digital encoder includes

a fine decoder that converts the set of digitized fine signals into the least significant bits of the digital signal by determining a number corresponding to the number of the set of digitized fine signals having a first logic level and setting the least significant bits equal to the number, and

a course decoder that converts the set of digitized course signals to the most significant bits of the digital signal by determining a course number indicating the number of the set of digitized course signals having a second logic level.

202. The digital display unit of Claim 201, wherein whether the first logic level is the same or opposite the second logic level is determined by a voting circuit, the voting circuit determining if a region corresponding to the analog input signal is in a rising or falling section.

203. The digital display unit of Claim 202, wherein the voting circuit inputs one digit from a first extreme of the set of digitized fine signals and two digits from a second extreme opposite the first extreme of the set of digitized fine signals and determines whether the region is a rising or falling section by 2/3 majority vote.

204. The digital display unit of Claim 201, wherein whether the first logic level is the same or opposite the second logic level is determined by the course number.

205. The digital display unit of Claim 201, wherein the digital decoder further includes an error correction circuit.

206. The digital display unit of Claim 205, wherein the error correction circuit inputs a determination of whether a region corresponding to the analog input signal is in a rising or falling section, the least significant bit of the course number, and the next to most significant bit of the fine number, determines if there is an agreement of whether the region is a rising or falling section, and adjusts the course number if there is no agreement.

207. The digital display unit of Claim 201, wherein the digital decoder further includes a range correction circuit.

208. The digital display unit of Claim 207, wherein the range correction circuit inputs a first signal of the set of digitized fine signals and a second signal of the set of digitized fine signals, the first signal and the second signal being chosen to be near end points of a range of allowed differential input signals, and the most significant bit of the digital signal, the range correction circuit sets the digital signal at a high extreme value if the first signal indicates a high value of the analog input signal and the most significant bit of the digital signal is not one and sets the digital signal at a low extreme value if the second signal indicates a low value of the analog input signal and the most significant bit of the digital signal is not 0.

209. A digital display unit, comprising:

an array of pixels;

a digital pixel controller coupled to the array of pixels, the digital pixel controller capable of turning on pixels in the array of pixels in response to a set of digital video signals; and

a graphics digitizer coupled to the digital pixel controller, the graphics digitizer supplying the set of digital video signals in response to a set of analog video signals, the graphics digitizer including

at least one channel, each of the at least one channel inputs an analog video signal and outputs a digital video signal;

a phase-locked-loop coupled to a horizontal sync signal, the phase-locked-loop providing a sampling clock frequency to the at least one channel; and

a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency and outputs a synchronized horizontal sync signal consistent with the sampling clock frequency and the digital video signal,

wherein each of the at least one channel includes an analog-to-digital converter coupled to receive the analog video signal, the analog-to-digital converter comprising:

a sample and hold circuit that receives an analog input signal and outputs a differential input signal in response to a sampling clock signal;

a reference generator that receives a reference voltage and generates a set of differential reference signals;

a pre-amp bank that receives the differential input signal from the sample and hold circuit and the set of differential reference signals from the reference generator and outputs a set of differential output signals indicative of a comparison between the differential input signal and the set of differential reference signals;

a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals;

a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals;

a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals; and

a digital encoder that receives the set of digitized fine signals and the set of digitized course signals and outputs a digital signal indicative of the analog input signal,

wherein the set of differential reference signals includes 32 reference signals and the set of differential output signals includes 32 output signals.

210. The digital display unit of Claim 209, wherein the set of differential folded signals includes 32 differential folded signals.

211. The digital display unit of Claim 210, wherein the set of differential course output signals includes 7 differential course output signals.

212. The digital display unit of Claim 211, wherein the digitized signal includes 8 bits.

213. A method of generating a programmable sampling clock frequency, comprising:

receiving a reference signal;

comparing the phase of the reference signal with a comparison signal and generating a control signal;

generating the programmable sampling clock frequency in response to the control signal;

generating the comparison signal in a programmable Div/N circuit, the frequency of the comparison signal being the programmable sampling clock frequency divided by a programmable number.

214. A method of generating a synchronized horizontal sync signal in a graphics digitizer, comprising:

sampling a horizontal sync signal with a phase-0 signal to form a local horizontal sync signal;

determining whether a programmable phase is within half a sampling clock cycle from the phase-0 signal;

sampling the local horizontal sync signal with sampling clock signal or with the complement of the sampling clock signal depending on whether the programmable phase is within half a sampling clock cycle from the phase-0 signal.

215. A method of generating a reference signal and a bias signal for an analog-to-digital converter, comprising:

generating a reference voltage proportional to a bandgap voltage in response to a reference value stored in a reference register;

generating a bias voltage proportional to the reverence value in response to an offset value stored in an offset register.

216. A method of offset canceling and resetting differential amplifiers in a pre-amp bank of an analog-to-digital converter, comprising coupling inputs of each differential amplifier of the pre-amp bank to a respective one of a set of reference voltage at the end of each video line.

217. A method of offset canceling and resetting differential amplifiers in a pre-amp bank of an analog-to-digital converter, comprising

selecting a set of differential amplifiers to be offset canceled and reset during a clock cycle; and

coupling inputs of the set differential amplifiers of the pre-amp bank to respective ones of a set of reference voltage.

218. A method of folding and interpolating a set of differential signals in an analog-to-digital converter, comprising:

actively averaging selected ones of a set of differential signals at the inputs of a first folding circuit and resistively interpolating to provide folded output signals; and

resistively interpolating in a second folding circuit that receives the folded output signals of the first folding circuit to provide a set of folded output signals.